An Analysis on a Pseudo-Differential Dynamic Comparator with Load Capacitance Calibration

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Abstract

This paper analyzes a pseudo-differential dynamic comparator with a dynamic pre-amplifier. The transient gain of a dynamic pre-amplifier is derived. This analysis enhances understanding of the roles of a transistor's parameters in a pre-amplifier's gain. Based on the calculated gain, a load capacitance calibration method is analyzed. The analysis helps designers' estimation for the accuracy of the calibration and the influence of PVT variation. The analyzed comparator uses 90-nm CMOS technology as an example and each estimation is compared with the simulation results.

1. Introduction

A comparator is the essential building block in an ADC to convert an analog signal into a digital signal. To suppress its power dissipation, recently published researches have used dynamic comparators [1]-[3]. Since the current flows only when they are triggered, they are more power efficient than comparators dissipating static current. However, this topology, an inverter chain, has deficiency, because, regeneration depends on the gain of an inverter—or the intrinsic gain of a transistor—, and as process is scaled down, its accuracy will become worse.

To address this issue, a latch with a dynamic amplifier, whose gain is approximately 5 times in 65-nm process [4], is proposed by D. Schinkel, *et al*. in 2007 [5]. However, this requires two phase of latching clocks. In 2008, We proposed a modified version of the double-tail latch comparator [6]. We removed the tail current of the second stage, which was triggered by inverse phase of a latching clock, and generated a trigger signal by using the outputs of a pre-amplifier. This modification can suppress the influence of skew between two phases of latching clocks in [6]. However, both comparators suffer kick-back noise. To suppress the kick-back noise, in 2010, pseudo-differential topology was introduced [7].

Those comparators with calibration circuits should be analyzed for their characteristics and optimizations. Thermal noise [4], [8]-[12] and mismatch [13] analysis methods about a dynamic comparator were already reported. In this paper, a load capacitance calibration method [2], [3] for a pseudo-differential dynamic comparator will be analyzed in 90-nm process. The gain of a dynamic amplifier will also be deduced for this analysis.

2. Comparator under Analysis

A pseudo-differential dynamic comparator will be briefly analyzed in this section. Its schematic is described in figure 1. The comparator is comprised of two stages. The first stage is a dynamic amplifier, or a pre-amplifier, which integrates differential input signals as time passes. The second stage actually performs the regeneration. In this paper, the size of all transistors are designed as 2 μm/100 nm.

Before analyzing the comparator, we describe its transient performance. As shown in figure 2, when CLK_{Latch} is low, M_5 and M_6 are on while M_3 and M_4 are off. Then, parasitic capacitors on nodes Out_{p_int} and Out_{n_int} are charged up to supply voltage. The second stage is turned off, because M_{15} and M_{16} are off. After CLK_{Latch} becomes high, M_3 and M_4 are on; while M_5 and M_6 are off. Accordingly, electric charge on the node Out_{p_int} and Out_{n_int} flows into *gnd*. Drain currents of M_3 and M_4 are determined by input signals of M_1 and M_2. Differences of flowing electric charge per time at the nodes Out_{p_int} and Out_{n_int} induces a voltage difference at the nodes, and the voltage difference becomes larger as time passes. If voltages on the node Out_{p_int} and Out_{n_int}

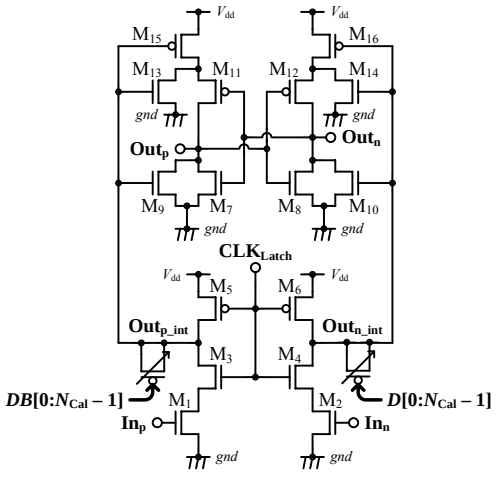


Figure 1. A pseudo-differential dynamic comparator with load capacitance calibration

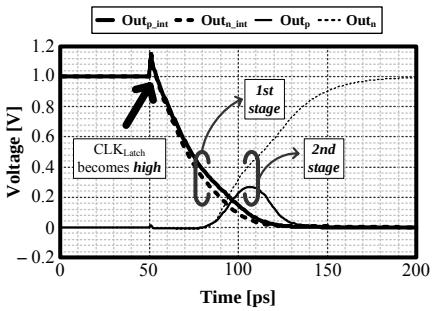


Figure 2. Transient waveform of a comparator

drop sufficiently, then the second stage regenerates the voltage difference between node Out_{p_int} and Out_{n_int}.

To simplify the analysis, we set the rising time of CLK_{Latch} to 1 ps as the simulation condition and M_3 and M_4 are in the deep triode region when CLK_{Latch} is high. When M_3 (or M_4) is in the deep saturation region, V_{out_int} which is voltage of node Out_{int} can be approximated as the drain voltage of M_1 (or M_2).

2.1 Gain of a Dynamic Amplifier

A pre-amplifier increases the difference between the differential input signals. To figure out its gain, G_{amp}, let us simplify the first stage of a dynamic comparator when CLK_{Latch} is high as depicted in figure 3. The output of a pre-amplifier is described as below;

$$V_{out\_int} = V_{dd} - \frac{I_{DS}}{C}t \tag{1}$$

where I_{DS} is the drain current of the input transistors, C is the total load capacitance on its output node, and t is the integration time. I_{DS} with channel-length modulation is expressed as below;

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{eff}^2\left(1+\lambda\left(V_{DS}-V_{DS\_sat}\right)\right) \tag{2}$$

$$V_{eff} \equiv V_{GS} - V_{th} \tag{3}$$

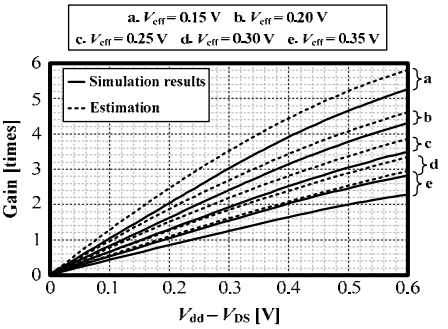
where V_{DS_sat} is the saturation condition of drain-source voltage, which equals V_{eff}, and λ indicates the channel-length modulation coefficient. When V_{out_int} is decreased from V_{dd} to V_{DS}, average drain current, $\overline{I_{DS}}$, is expressed as below;

$$\begin{aligned}\overline{I_{DS}} &= \frac{1}{V_{dd}-V_{DS}}\int_{V_{DS}}^{V_{dd}} I_{DS}\mathrm{d}V_{DS} \\ &= \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{eff}^2\times\left(1+\frac{\lambda}{2}\left(V_{dd}+V_{DS}-2V_{eff}\right)\right)\end{aligned} \tag{4}$$

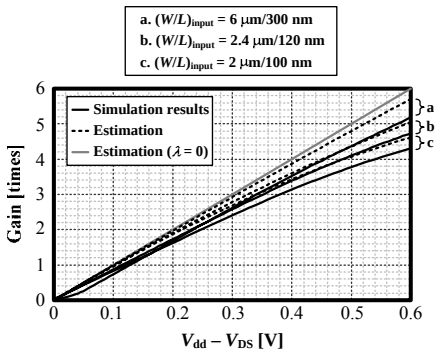
Substituting equation (4) into equation (1), then the integration time can be represented as;

$$t = \frac{\left(V_{dd}-V_{DS}\right)C}{\overline{I_{DS}}}. \tag{5}$$

From equation (2), transconductance, g_m, and a signal current due to g_m, i_{DS1}, are expressed as below;



(a) various V_{eff}



(b) various channel length when V_{eff} is 0.2 V

Figure 3. Gain of a pre-amplifier

$$g_m = \mu C_{OX}\frac{W}{L}V_{eff}\left(1+\lambda\left(V_{DS}-V_{DS\_sat}\right)\right) \tag{6}$$

$$i_{DS1} = g_m v_{in} \tag{7}$$

where v_{in} is an input signal. From the equation (2), small signal output conductance, g_{DS}, and a signal current due to g_{DS}, i_{DS2}, are expressed as below;

$$g_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{eff}^2\lambda \tag{8}$$

$$i_{DS2} = g_{DS} v_{out} \tag{9}$$

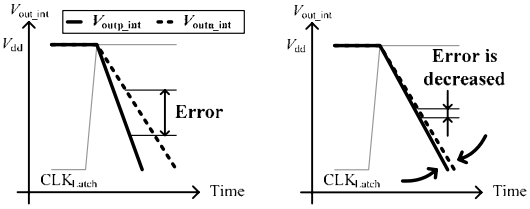
where v_{out} is an output signal integrated on a load capacitor. Substituting equations (4) and (5) into equation (1), then an output differential signal, v_{out_diff}, of a pre-amplifier is deduced;

$$\begin{aligned} v_{out\_diff} &\equiv V_{outp\_int}(t) - V_{outn\_int}(t) \\ &= -\frac{2\left(V_{dd}-V_{DS}\right)}{V_{eff}}v_{in\_diff}\end{aligned} \tag{10}$$

where v_{in_diff} is an input differential signal, $2v_{in}$. Substituting equation (10) into equation (9), then

$$i_{DS2} = -g_{DS}\frac{2\left(V_{dd}-V_{DS}\right)}{V_{eff}}v_{in}. \tag{11}$$

As shown in equation (11), the signal current due to g_{DS} has the opposite sign of v_{in} and attenuates an integrated output signal by g_m. i_{DS2} becomes larger as the integrated output signal increases—or V_{out_int} decreases from V_{dd}.



(a) before calibration (b) after calibration

Figure 4. Error reduction by calibration

When the total signal current, i_{DS}, is a sum of i_{DS1} and i_{DS2}, then the average total signal current is

$$\begin{aligned}\overline{i_{DS}} &= \frac{1}{t}\int_0^t i_{DS}\mathrm{d}t = \frac{1}{V_{DS}-V_{dd}}\int_{V_{dd}}^{V_{DS}} i_{DS}\mathrm{d}V_{DS} \\ &= \mu C_{OX}\frac{W}{L}V_{eff}\left(1+\lambda\left(V_{DS}-V_{eff}\right)\right)\times v_{in} \\ &= g_{m\left(V_{out\_int}=V_{DS}\right)}v_{in}\end{aligned} \quad (12)$$

From equations (1) and (12), transient gain, G_{amp_trans}, is expressed as below;

$$\begin{aligned}G_{amp\_trans} &= \frac{v_{out}}{v_{in}} = -\frac{\overline{i_{DS}}t}{Cv_{in}} \\ &= -\frac{2\left(V_{dd}-V_{DS}\right)}{V_{eff}}\times\frac{1+\lambda\left(V_{DS}-V_{eff}\right)}{1+\frac{\lambda}{2}\left(V_{dd}+V_{DS}-2V_{eff}\right)}.\end{aligned} \quad (13)$$

Equation (13) is compared with simulation results in figure 3. Equation (2) is satisfied only when V_{out_int} is larger than V_{eff}. If V_{out_int} falls to V_{eff}, G_{amp_trans} reaches its maximum.

3. Load Capacitance Calibration

The load capacitance calibration [2], [3] changes the load capacitance where a signal is integrated as depicted in the figure 1. From equation (1), the slew rate, I_{DS}/C, is inversely proportional to the load capacitance. When the calibration is conducted, these slew rates become closer together and the offset voltage is compensated as described in figure 4.

3.1 Input-Referred Compensated Voltage

Based on equation (1), let us estimate the input-referred compensated voltage of the capacitance calibration. First, differentiate equation (1) with respect to capacitance;

$$\frac{\mathrm{d}V_{out\_int}}{\mathrm{d}C} = \frac{V_{dd}-V_{DS}}{C}. \quad (14)$$

Assuming an input signal of the second stage is decided when gain reaches its maximum, input-referred variation is deduced as below;

$$\begin{aligned}v_{in\_diff\_cal} &= -\frac{V_{eff}}{C}\left(1+\frac{\lambda}{2}\left(V_{dd}-V_{eff}\right)\right) \\ &\times\left(N_{Code}-2^{N_{cal}-1}\right)\times\left(C_{on}-C_{off}\right)\end{aligned} \quad (15)$$

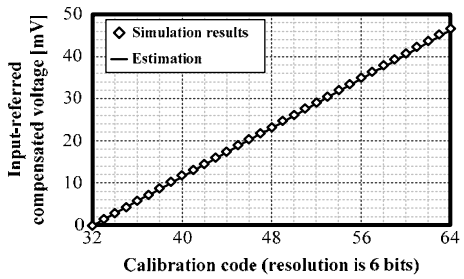


Figure 5. Input-referred compensated voltage by the capacitance calibration

(V_{dd} = 1.0 V, V_{in_com} = 0.5 V, calibration resolution is 6 bits, and unit PMOS capacitor size is W/L = 600 nm/100 nm)

where C_{on} and C_{off} are the capacitances of a unit-sized varactor which is turned on and off, respectively, N_{Code} is the calibration code, N_{cal} is the calibration resolution, and $v_{in\_diff\_cal}$ is the input-referred compensated voltage in differential. Figure 5 compares equation (15) with the simulation results.

3.2 PVT Variation

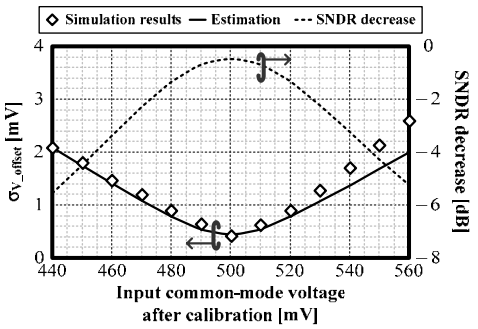
PVT variation degrades compensation accuracy. Influence of the process is fixed in the factory and this doesn't affect the offset after calibration. Only voltage fluctuation and temperature change are considered. From equation (13), G_{amp_tran} is decided by a ratio of V_{dd} to V_{eff} and λ. If temperature is changed, then V_{th} and λ are varied. Influence of voltage fluctuation is easy to understand. From equation (15), input-referred compensated voltages also change and the variation differs in each calibration code. If error due to PVT variation, σ_{V_PVT}, is uncorrelated with offset after calibration, $\sigma_{V\_offset0}$, then total offset voltage, σ_{V_offset}, can be expressed as

$$\sigma^2_{V\_offset} = \sigma^2_{V\_offset0} + \sigma^2_{V\_PVT}. \quad (16)$$

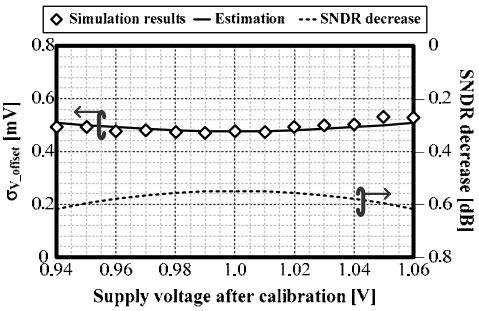
From equation (15), when standard deviation of calibration code is σ_{Code}, σ_{V_PVT} due to input common-mode voltage, $\sigma_{V\_PVT\_Vcom}$, is deduced as below;

$$\begin{aligned}\sigma_{V\_PVT\_VCOM} &= \frac{V_{eff}}{C}\left(1+\frac{\lambda}{2}\left(V_{dd}-V_{eff}\right)\right) \\ &\times\left(\left(\frac{\Delta V_{eff}}{V_{eff}}-\frac{\lambda\Delta V_{eff}}{2+\lambda\left(V_{dd}-V_{eff}\right)}\right)^2+\left(\frac{\left(V_{dd}-V_{eff}\right)\Delta\lambda}{2+\lambda\left(V_{dd}-V_{eff}\right)}\right)^2\right)^{\frac{1}{2}}\left(C_{on}-C_{off}\right)\sigma_{Code}.\end{aligned} \quad (17)$$

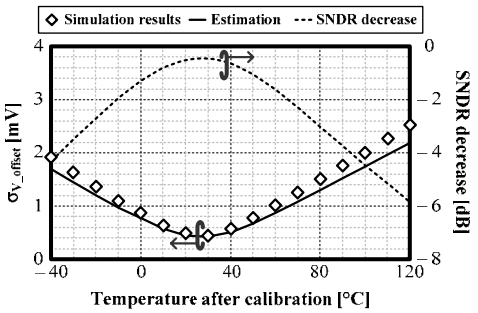
Influences of supply voltage and temperature can be deduced by the same way. Figure 6 compares the estimation with the simulation results. Calibration is conducted when V_{dd} is 1.0 V, V_{in_com} is 0.5 V, and T is 27 °C. Figure



(a) input common-mode voltage



(b) supply voltage



(c) temperature

Figure 6. Influence of PVT variation on the capacitance calibration

(1 LSB = 4.5 mV and a number of simulation is 500)

6 also shows SNDR decrease which is calibrated from estimated σ_{V_PVT}. Assuming an input signal is a sine wave and the architecture of an ADC is flash, SNDR decrease is expressed as

$$\begin{aligned} \mathrm{SNDR}_{\mathrm{decrease}} &= \mathrm{SNDR} - \mathrm{SQNR} \\ &= -10\log\left(1+\frac{12}{V_{\mathrm{q}}^2}\sigma_{\mathrm{V}}^2\right) \end{aligned} \qquad (18)$$

where V_q is 1 LSB. In figure 6, V_q is supposed to be three times of the least changeable voltage in calibration which equals 4.5 mV.

4. Summary

This work analyzed a pseudo-differential dynamic comparator with load capacitance calibration. The analyzed comparator uses 90-nm CMOS process as an example. The gain of a dynamic amplifier was expressed by a ratio of V_{dd} to V_{eff} and λ of an input transistor. Based on the deduced gain, input-referred compensate voltage and influence of PVT variation are analyzed and compared with the simulation results.

Acknowledgments

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